

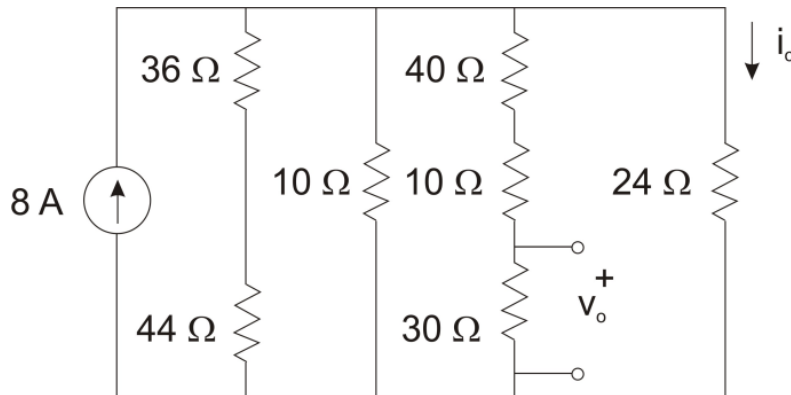
FYSE301 Elektronikka I osa A

Loppukoe 27.4.2012 Vastaa kaikkiin viiteen kysymykseen

1. Selitä lyhyesti

- Theveninin teoreema (2 p)
- Itseispuolijohde ja seostettu puolijohde. (2 p)
- Piirrä p-kanava JFETin rakenne (poikkileikkauskuva riittää) ja nimeä transistorin osat (2 p)

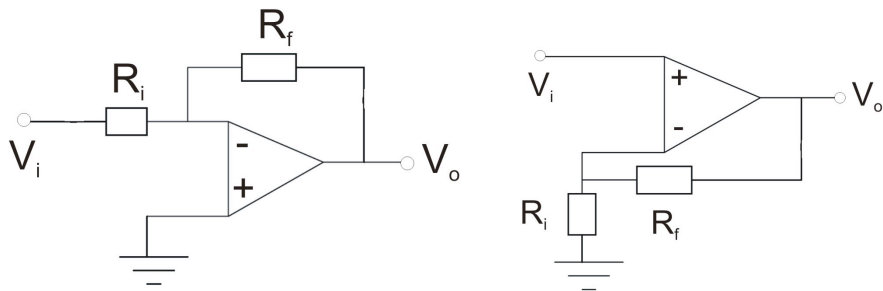
2. Laske virta i_o ja jännite v_o kuvan 1 piirissä



Kuva 1.

3. a) Kuvaile ideaalisen operaatiovahvistimen ominaisuudet lyhyesti (2 p)

b) Kuvassa 2 on esitetty invertoivan ja ei-invertoivan vahvistimen kytkennät. Määritä vahvistus V_o / V_i kummallekin piirille (voit olettaa operaatiovahvistimet ideaalisiksi ja että niiden navat ovat virtuaalisessa oikosulussa). (4 p)

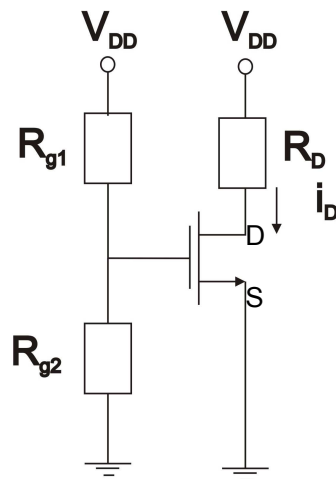


Invertoiva vahvistin

Ei-invertoiva vahvistin

Kuva 2

4. Kuva 3 esittää MOSFET-transistorin biasointikytkentää, jolla lepotilan toimintapiste asetetaan halutuksi. Oletetaan että piirissä on BS170 NMOS transistori (liite).
- (a) Piirrä avaustyyppin (enhancement mode) NMOS-transistorin poikkileikkaus, josta selviää transistorin toimintaperiaate. Nimeä transistorin osat. (2 p)
- (b) Määritä liitteen tiedoista mikä on i) hilan (gate) kynnyksjännite, ii) virta I_D kun $V_{GS}=0$ V ja $V_{DS}=25$ V (2 p)
- (c) Olkoon kuvan 4 mukaisessa kytkennässä $V_{DD} = 29$ V ja $R_D = 10$ W. Määritä nieluvirta (I_D) ja nielu-lähdejännite (V_{DS}), kun $V_{GS} = 6$ V. Kuinka hilavastukset on valittava jotta saadaan $V_{GS} = 6$ V? Käytä apuna liitettä, jos siltä tuntuu. (2 p)

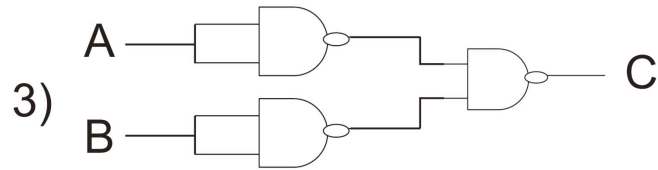
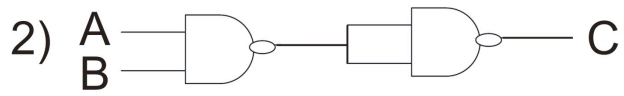
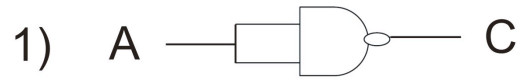


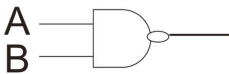
Kuva 3.

5. a) Kuvassa 4 on esitetty kolme erilaista NAND-porteista koostuvaa piiriä. Määritä kunkin piirin anto C kaikilla A:n ja B:n arvoilla. Minkä loogisen operaation kukin piiri suorittaa? Mikä ominaisuus NAND-portilla on laskemiesi tulosten perusteella? (3 p)
- b) Kuvaile sanallisesti ja kuvia apuna käyttäen tyhjennysalueen muodostuminen pn-rajapinnan läheisyyteen. (3 p)

Joitain kenties hyödyllisiä yhtälöitä:

$$\sigma = ne\mu; n = p = n_i; n_i = e^{-E_g/2kT}; i = I_s(e^{eV/\eta kT} - 1); i_D = K(V_{GS} - V_T)^2; i_D = I_{DSS}(1 - V_{GS}/V_P)^2; \beta = \alpha/(1 - \alpha);$$



	<table border="1"><thead><tr><th>A</th><th>B</th><th>$\overline{A \cdot B}$</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></tbody></table>	A	B	$\overline{A \cdot B}$	0	0	1	0	1	1	1	0	1	1	1	0
A	B	$\overline{A \cdot B}$														
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Kuva 4

BS170 / MMBF170 N-Channel Enhancement Mode Field Effect Transistor

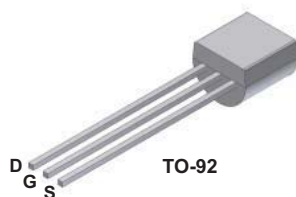
General Description

These N-Channel enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching performance. They can be used in most applications requiring up to 500mA DC. These products are particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

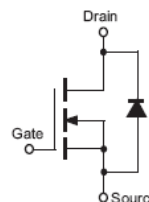
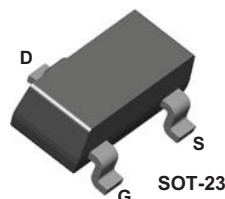
Features

- High density cell design for low $R_{DS(ON)}$.
- Voltage controlled small signal switch.
- Rugged and reliable.
- High saturation current capability.

BS170



MMBF170



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	BS170	MMBF170	Units
V_{DSS}	Drain-Source Voltage	60		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1M\Omega$)	60		V
V_{GSS}	Gate-Source Voltage	± 20		V
I_D	Drain Current - Continuous	500	500	mA
	- Pulsed	1200	800	
T_J, T_{STG}	Operating and Storage Temperature Range	- 55 to 150		$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 Seconds	300		$^\circ\text{C}$

Thermal Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	BS170	MMBF170	Units
P_D	Maximum Power Dissipation	830	300	mW
	Derate above 25°C	6.6	2.4	mW/ $^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	150	417	$^\circ\text{C}/\text{W}$

Electrical Characteristics $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Conditions	Type	Min.	Typ.	Max.	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 100\mu A$	All	60			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 25V, V_{GS} = 0V$	All			0.5	μA
I_{GSSF}	Gate - Body Leakage, Forward	$V_{GS} = 15V, V_{DS} = 0V$	All			10	nA
ON CHARACTERISTICS (Notes 1)							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 1mA$	All	0.8	2.1	3	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10V, I_D = 200mA$	All		1.2	5	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 10V, I_D = 200mA$	BS170		320		mS
		$V_{DS} \geq 2 V_{DS(on)}, I_D = 200mA$	MMBF170		320		
Dynamic Characteristics							
C_{iss}	Input Capacitance	$V_{DS} = 10V, V_{GS} = 0V, f = 1.0MHz$	All		24	40	pF
C_{oss}	Output Capacitance		All		17	30	pF
C_{rSS}	Reverse Transfer Capacitance		All		7	10	pF
Switching Characteristics (Notes 1)							
t_{on}	Turn-On Time	$V_{DD} = 25V, I_D = 200mA, V_{GS} = 10V, R_{GEN} = 25\Omega$	BS170			10	ns
		$V_{DD} = 25V, I_D = 500mA, V_{GS} = 10V, R_{GEN} = 50\Omega$	MMBF170			10	
t_{off}	Turn-Off Time	$V_{DD} = 25V, I_D = 200mA, V_{GS} = 10V, R_{GEN} = 25\Omega$	BS170			10	ns
		$V_{DD} = 25V, I_D = 500mA, V_{GS} = 10V, R_{GEN} = 50\Omega$	MMBF170			10	

Note:

1. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2.0\%$.

Ordering Information

Part Number	Package	Package Type	Lead Frame	Pin array
BS170	TO-92	BULK	STRAIGHT	D G S
BS170_D26Z	TO-92	Tape and Reel	FORMING	D G S
BS170_D27Z	TO-92	Tape and Reel	FORMING	D G S
BS170_D74Z	TO-92	AMMO	FORMING	D G S
BS170_D75Z	TO-92	AMMO	FORMING	D G S
MMBF170	SOT-23	Tape and Reel		

Typical Electrical Characteristics

BS170 / MMBF170

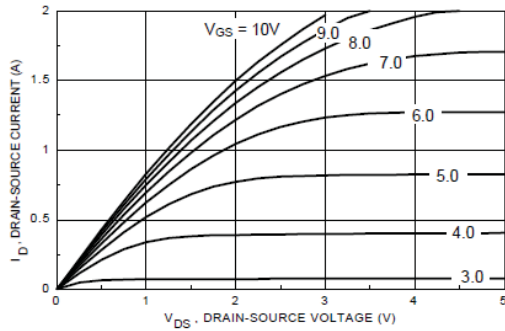


Figure 1. On-Region Characteristics.

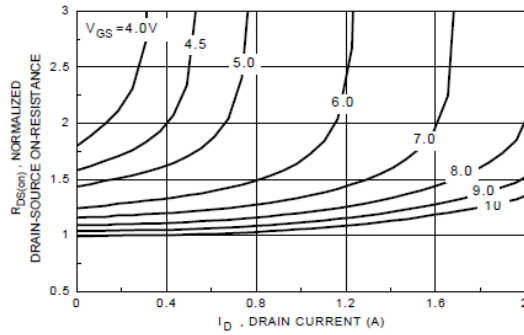


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

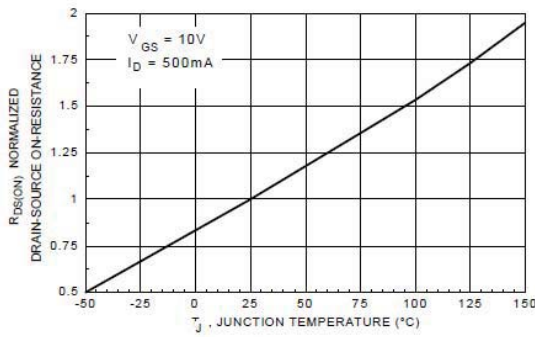


Figure 3. On-Resistance Variation with Temperature.

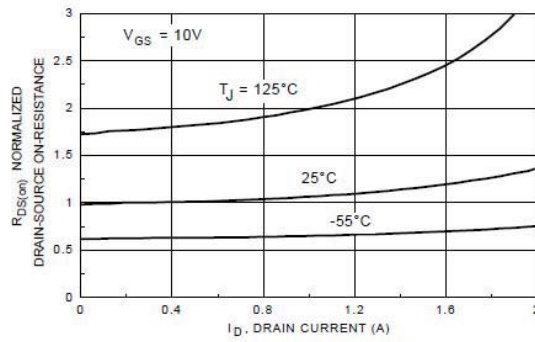


Figure 4. On-Resistance Variation with Drain Current and Temperature.

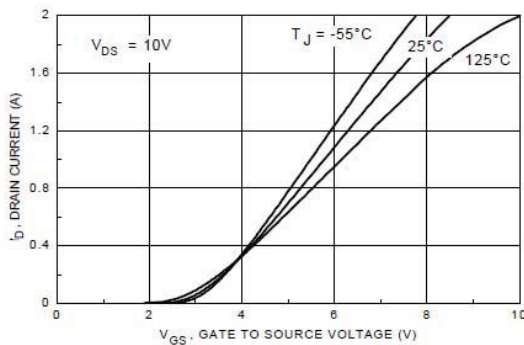


Figure 5. Transfer Characteristics.

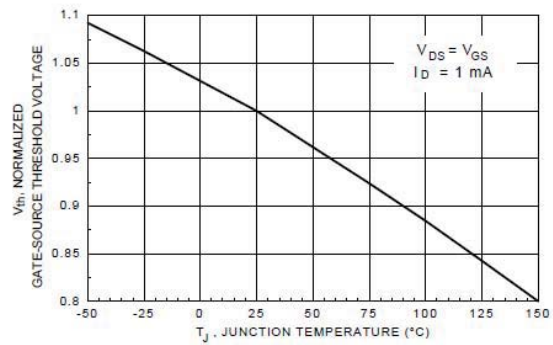


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

BS170 / MMBF170

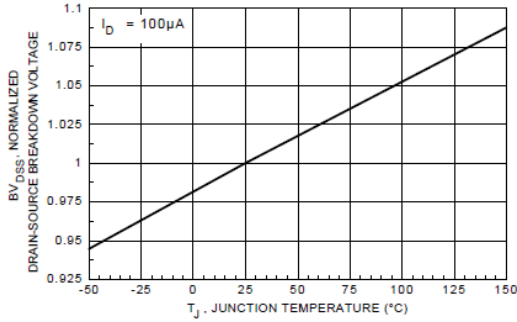


Figure 7. Breakdown Voltage Variation with Temperature.

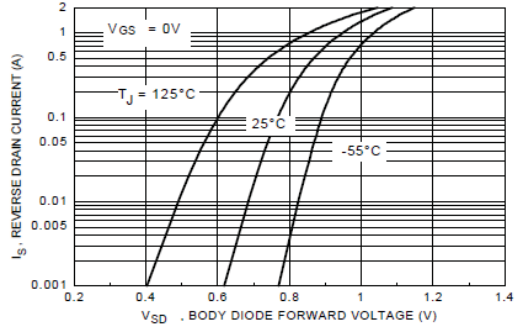


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

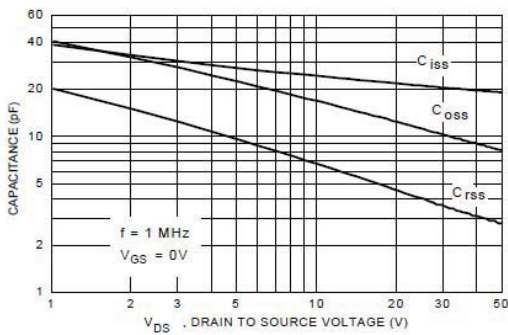


Figure 9. Capacitance Characteristics.

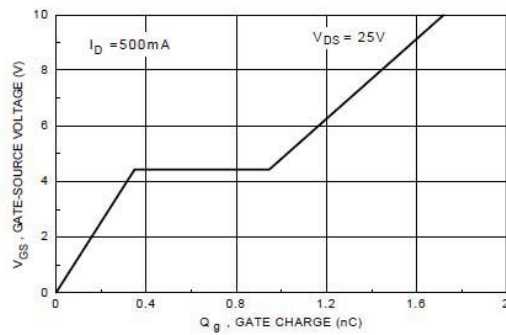


Figure 10. Gate Charge Characteristics.

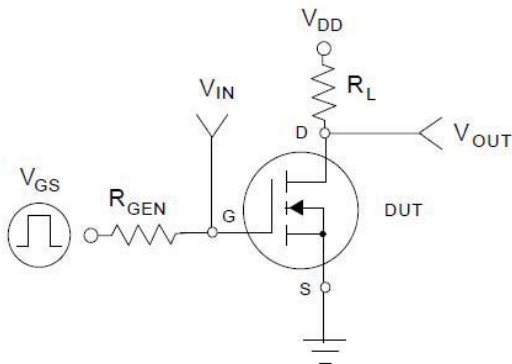


Figure 11. Switching Test Circuit.

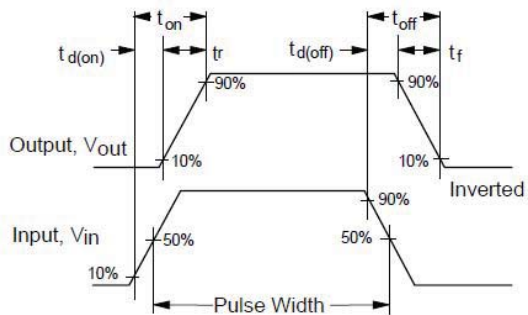


Figure 12. Switching Waveforms.

