FYSE301 Electronics 1A **Final exam 02/26/2010**

Time: 4 h **Examiner: Veikko Linko**

Answer all five (5) questions! Maximum points awarded are 5 x 6p = 30p.

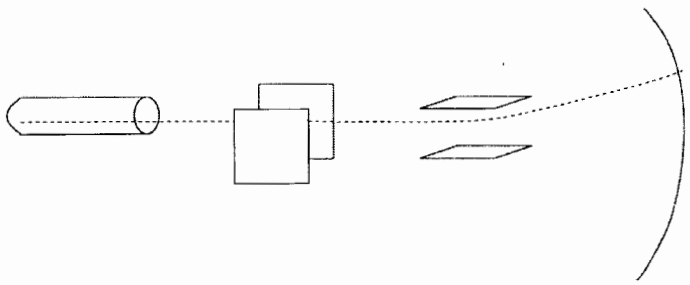
Return all your answering sheets! You may keep this exercise sheet.

1. **Explain shortly but understandably**

   a) The law of mass action ($np=n_i^2$) (2p)

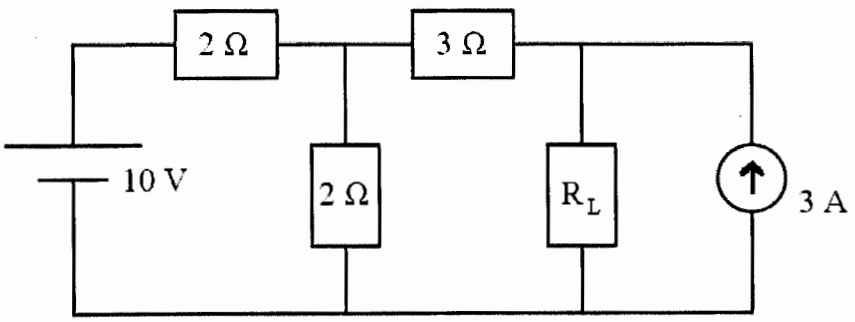
   b) The superposition principle in linear circuits (2p)

   c) Name the parts of the analog oscilloscope in the figure below and add the deflection voltages v_x and v_y to the picture. Explain to which part the signal is connected and how the time sweep is done. (2p)



2. **Linear circuits.**

   Form the Thevenin and Norton equivalents of the circuit below for the load resistance R_L. (6p)

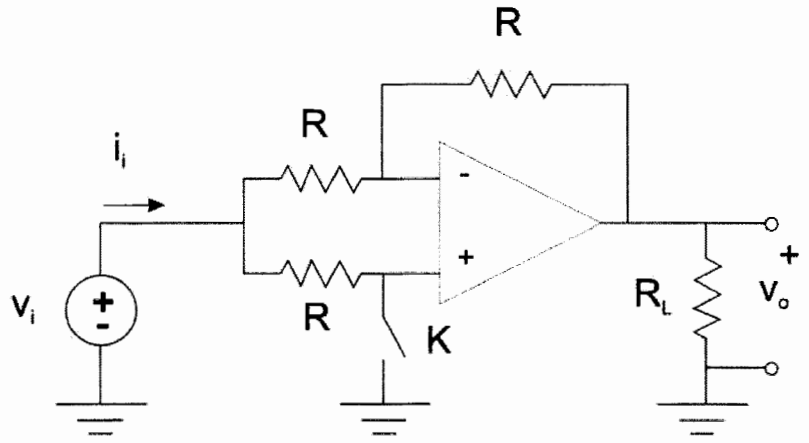


3. Operational amplifier.

Calculate the amplification $A = v_o / v_i$ and input resistance $R_i = v_i / i_i$ in the operational amplifier construct below when the switch K is

a) closed (conducting) (3p)

b) open (not conducting) (3p)



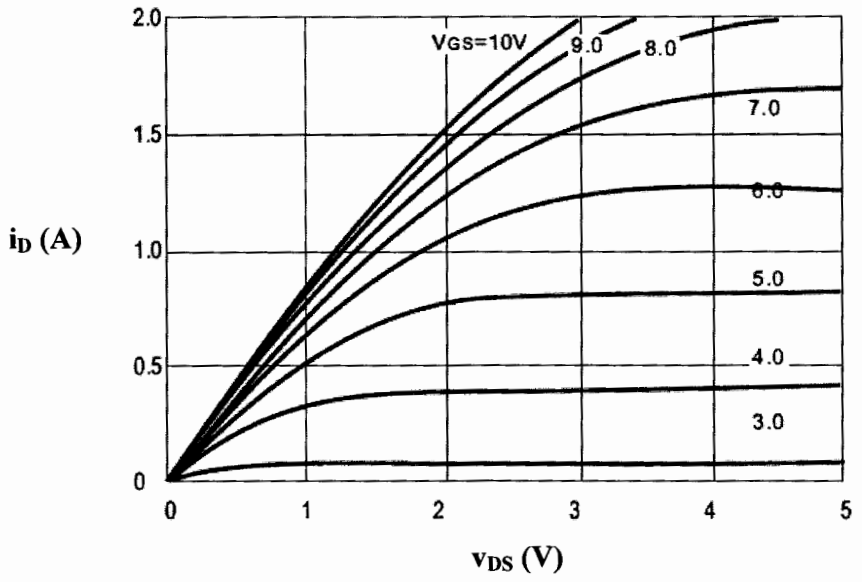
4. Semiconductors.

a) Explain how a depletion region is formed in the proximity of the pn-junction when it is not connected to a circuit. Start from the situation where p and n type semiconductors are brought to contact with each other. You may use figures as a part of your explanation. Sketch the charge density, electric field, and electric potential for the depletion region in the direction normal to the pn-interface. (4p)

b) How do the currents across the pn-junction caused by majority and minority charge carriers change, when an external voltage bias is connected across the junction? Consider both reverse and forward biases and sketch the total current through the pn-junction as a function of external voltage on the basis of your explanation. (2p)

5. Transistors.

a) Draw a cross section figure of the NMOS enhancement mode transistor. Name the semiconductor types and gate, source and drain in your figure. Explain the operating principle of the enhancement-mode NMOS and (qualitatively) the characteristic i_D-v_{DS} –curves below for different values of v_{GS}. (3p)



b) Calculate the emitter, collector and base potentials for the circuit below featuring a silicon-based npn bipolar junction transistor with $\beta = 50$ in a common-emitter configuration, and a silicon-based diode. (3p)