FYSE302 Electronics 1B
Final Exam 27.5.2011

1. Briefly explain/describe:
   (a) Dynamic resistance (2p)
   (b) Common mode rejection ratio (2p)
   (c) DA conversion (2p)

2. At the circuit shown in figure 1 $v_s(t) = 10\sqrt{2}\cos(\omega t)$ V. Determine the current flowing through the coil by using thévenin's theorem, when $\omega = 900$ Hz.

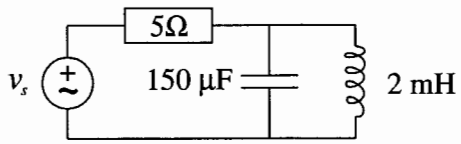


Figure 1:

3. The input resistance R_{in} of a voltage amplifier needs to be as high as possible, so that the amplifier does not induce much load on the other circuitry. A simple inverting amplifier circuit shown in figure 2(a) is not an ideal choice in this sense.
   (a) What is the highest possible input impedance $R_{\text{in}} = V_{\text{i}}/I_{\text{i}}$ for the circuit of figure 2(a), if the gain $V_{\text{o}}/V_{\text{i}}$ needs to be -100 and resistors higher than 1 MΩ are not allowed to use.
   (b) Better circuit is shown in figure 2(b). Choose the components so that the gain $V_{\text{o}}/V_{\text{i}} = -100$ and the input impedance $R_{\text{in}} = V_{\text{i}}/I_{\text{i}} = 1$ MΩ. Largest resistor allowed is 1 MΩ. (Resistors larger that 1 MΩ usually induce problems)

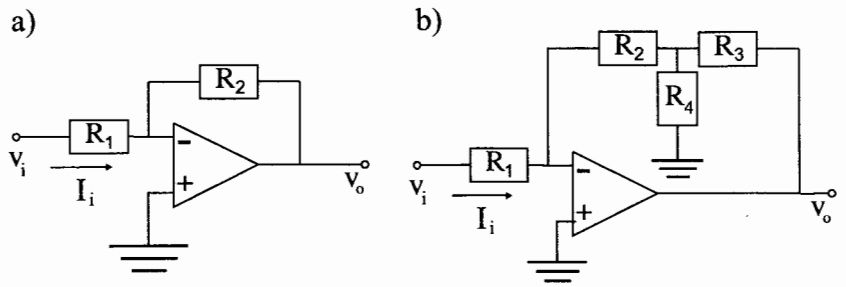


Figure 2:

4. The circuit presented in figure 3 is used as a power amplifier. The current amplification factor of a silicon transistor is $\beta = 100$. Furthermore, $V_{CC} = 15$ V, $R_1 = 10$ kΩ and $R_2 = 30$ kΩ

   (a) Choose R_E and R_C in such a way that the operation point of the transistor becomes $V_{CE} = 6$ V ja $I_C = 2$ mA.

   (b) Sketch the $i_C - v_{CE}$ –curves and draw the dc load-line in the same figure.

   Draw the ac load-line when $R_L = 3$ kΩ. Find out the ac-component of the output voltage v_o, when the input signal at the base is $i_b = 10\sin(\omega t)$ μA.

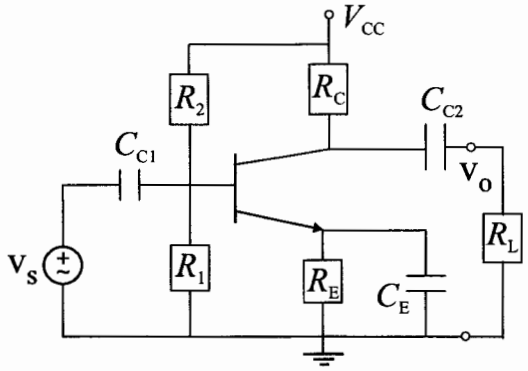


Figure 3:

5. Lets consider the circuit shown in Fig. 4, where $R_L = 8$ kΩ and $V_{GG} = 2$ V, and the values for the parameters describing the small-signal model of depletion field-effect MOSFET -transistor are $I_{DSS} = 10$ mA, $g_{m0} = 5000$ μS ja $r_d = 50$ kΩ. Determine I_D and choose V_{DD} so, that at the operation point $V_{DS} = 8$ V. Calculate the voltage amplification $|v_o/v_s|$ at this operation point using the small-signal model. Here v_s and v_o are the complex amplitudes of the small signals. For a MOSFET:

$$i_D = I_{DSS}\left(1 - \frac{v_{gs}}{V_P}\right)^2, \quad g_m = \frac{di_D}{dv_{GS}}$$

$$\text{and} \quad g_{m0} = \left.\frac{di_D}{dv_{GS}}\right|_{v_{GS}=0}$$

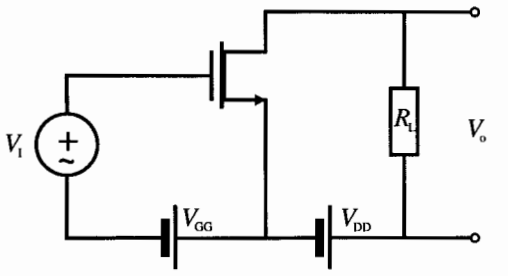
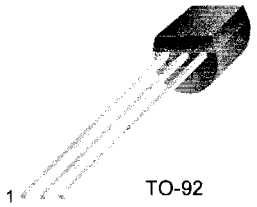


Figure 4:

FAIRCHILD
SEMICONDUCTOR®

PN2222

General Purpose Transistor



TO-92

1. Emitter 2. Base 3. Collector

NPN Epitaxial Silicon Transistor

Absolute Maximum Ratings T_a=25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{CBO}	Collector-Base Voltage	60	V
V_{CEO}	Collector-Emitter Voltage	30	V
V_{EBO}	Emitter-Base Voltage	5	V
I_C	Collector Current	600	mA
P_C	Collector Power Dissipation	625	mW
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-55 ~ 150	°C

Electrical Characteristics T_a=25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Max.	Units
BV_{CBO}	Collector-Base Breakdown Voltage	I_C=10μA, I_E=0	60		V
BV_{CEO}	Collector Emitter Breakdown Voltage	I_C=10mA, I_B=0	30		V
BV_{EBO}	Emitter-Base Breakdown Voltage	I_E=10μA, I_C=0	5		V
I_{CBO}	Collector Cut-off Current	V_{CB}=50V, I_E=0		0.01	μA
I_{EBO}	Emitter Cut-off Current	V_{EB}=3V, I_C=0		10	nA
h_{FE}	DC Current Gain	V_{CE}=10V, I_C=0.1mA V_{CE}=10V, *I_C=150mA	35 100	 300	
V_{CE} (sat)	* Collector-Emitter Saturation Voltage	I_C=500mA, I_B=50mA		1	V
V_{BE} (sat)	* Base-Emitter Saturation Voltage	I_C=500mA, I_B=50mA		2	V
f_T	Current Gain Bandwidth Product	V_{CE}=20V, I_C=20mA, f=100MHz	300		MHz
C_{ob}	Output Capacitance	V_{CB}=10V, I_E=0, f=1MHz		8	pF

* Pulse Test: Pulse Width≤300μs, Duty Cycle≤2%