## DIGITALELECTRONICS FYSE410

1. The transfer function of the inverter $A$ is described below. Derive the values of the parameter: $\mathrm{V}_{\mathrm{OH}}, \mathrm{V}_{\mathrm{OL}}, \mathrm{V}_{\mathrm{IH}}$ ja $\mathrm{V}_{\mathrm{IL}}$. Calculate also the values of the noise margins $\mathrm{NM}_{\mathrm{H}}$ and $\mathrm{NM}_{\mathrm{L}}$.


The inverter $A$ drive the inverter $B$. The values of the parameters $\mathrm{V}_{\mathrm{OH}}, \mathrm{V}_{\text {OL }}, \mathrm{V}_{\text {IH }} \mathrm{ja} \mathrm{V}_{\text {IL }}$ for the inverter B are given below. Does this connection work or not? And why.

$$
\mathrm{A} \quad \mathrm{~B}
$$



$$
\begin{aligned}
& \mathrm{V}_{\mathrm{OH}}=4.5 \mathrm{~V} \\
& \mathrm{~V}_{\mathrm{OL}}=1.7 \mathrm{~V} \\
& \mathrm{~V}_{\mathrm{IH}}=3 \mathrm{~V} \\
& \mathrm{~V}_{\mathrm{IL}}=2 \mathrm{~V}
\end{aligned}
$$

2. In the picture below is shown the circuit which drives LED. The parameters of TTL-inverter are :

$$
\begin{aligned}
V_{O L \max } & =0.4 \mathrm{~V} \\
V_{O H \min } & =2.4 \mathrm{~V}
\end{aligned}
$$



Determine resistance $\mathrm{R}_{\mathrm{C}}$, so that Q 1 is on the saturation regime $\left(\mathrm{V}_{\mathrm{CE}}=0.2 \mathrm{~V}\right)$, when Light Emitting Diode is "ON" ( $\mathrm{I}_{\mathrm{d}}=20 \mathrm{~mA}$ and $\mathrm{V}_{\mathrm{D}}=2 \mathrm{~V}$ ).
What is the maximum value for the $\mathrm{R}_{\mathrm{B}}$, which keeps transistor Q 1 in saturation, when inverters output voltage is $\mathrm{V}_{\mathrm{OH}}=2.4 \mathrm{~V}$. Use value 0.8 V for the $\mathrm{V}_{\mathrm{BE}}$ on saturation. Power supply voltage $\mathrm{V}_{\mathrm{C}}=5 \mathrm{~V}$.
3. Design the kombinational logic for the Boolean function $f_{3}$ with minimum number of logic gates. Use only one type of 2-input gates. Draw the circuit diagram.

$$
f_{3}(D, C, B, A)=\sum(0,1,2,3,5,7,8,9,10,11,13,15)
$$

4. Implement the synchronous counter described in the state diagram given below. Use only T flip-flops. Outputs are $Q_{0}$ up to $Q_{3}$ are output (Q) of T-ffs. Draw only clock connections between T -ffs and give minimized Boolean functions for each exitation functions of ffs. Counter must be a self starting type.

5. Design the synchronous counter to generate two nonowerlapped clocks $\mathrm{Q}_{0}$ and $\mathrm{Q}_{1}$. The outputs $\mathrm{Q}_{0}$ and $\mathrm{Q}_{1}$ are also the outputs of the used D-flip flops of the counter. The counter should be the self starting. (The number of D-flip flops can be different than the number of outputs).


Use begin state A as a trap state. Give only Boolean functions for excitation functions of D-flip-flops and draw clock connections between D-ffs.
6. Explain shortly : implementing complex Boolean functions with pull-up/pulldown networks (CMOS-logic).

Implement the Boolean function shown below. Use symbols of $n$ - and p-type mosfets given below.

$$
Y=(\bar{A}+\bar{B})(\bar{C} \cdot \bar{D}+\bar{B})
$$



